Docket: 8021-160 (SS-18118-US)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Sun, et al. Examiner: Thanh V. Pham

Serial No.: 10/621,292 Group Art Unit: 2823

Filed: July 17, 2003
For: **METHOD OF FABRICATING SEMICONDUCTOR DEVICE USING A NICKEL SALICIDE PROCESS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

In response to the Final Office Action dated April 3, 2007 rejecting claims 1, 2, 5-8, 12 13, 16-19, 22, 23, and 26-31 under 35 U.S.C. § 103 (a) and the advisory Action dated June 13, 2007, Applicants appeal pursuant to the Notice of Appeal dated July 19, 2007, and respectfully submits this appeal brief.

TABLE OF CONTENTS

1. REAL PARTY IN INTEREST

The real party in interest is Samsung Electronics Co., Ltd, by virtue of assignment dated June 30, 2003 and recorded July 17, 2003 in the United States Patent and Trademark Office at reel 014309 and frame 0465 for the subject application.

2. RELATED APPEALS AND INTERFERENCES

None.

3. STATUS OF THE CLAIMS

Claims 1, 2, 5-8, 12 13, 16-19, 22, 23, and 26-31 are pending and stand rejected. Claims 1, 2, 5-8, 12 13, 16-19, 22, 23, and 26-31 are under appeal. A copy of the claims under appeal is presented in the Claims Appendix attached herewith.

4. STATUS OF THE AMENDMENTS

No amendments were filed in response to the Final Office Action in this case.

5. SUMMARY OF CLAIMED SUBJECT MATTER

It is to be understood that the following description of the claimed subject matter and references to the specification and drawings are for illustrative purposes only to provide some context for the claimed subject matter, but shall not be construed as placing any limitations thereon or limiting the scope thereof.

Methods for fabricating a semiconductor device are provided and claimed. As set forth in claim 1, a method for fabricating a semiconductor device comprises forming a gate pattern and a source/drain region on a silicon substrate (See Application at page 4, lines 9-13 and 20-21, and Figs 2A at reference numerals 19, 23 and 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed (See Application at page 5, lines 1-2, and Figures 2B at reference numerals 25, 11, 19 and 23), forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the

nickel alloy for silicide (See Application at page 5, lines 7-8 and Figures 2B at reference numerals 27, 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region (See Application at page 5, lines 20-23 and Figure. 2C at reference numerals 25, 27, 29, 19 and 23), and selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region (See Application at page 5, lines 28-31, page 6, lines 1-5 and Figure 2D at reference numerals 25, 27, 29, and 23) and whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

As set forth in claim 12, a method for fabricating a semiconductor device comprises forming a field region on a substrate to define an active region (See Application at page 4, lines 9-10 and Figure 2A at reference numerals 13 and 11), forming a gate pattern on the active region, wherein the gate pattern includes sidewalls (See Application at page 4, lines 11-15 and Figure 2A at reference numerals 19 and 13), forming spacers on the sidewalls of the gate pattern (See Application at page 4, lines 15-19 and Figure 2A at reference numerals 21 and 19), forming source/drain regions aligned with the spacers on both sides of the gate pattern (See Application at page 4, lines 20-21 and Figure 2A at reference numerals 21 and 19), cleaning the substrate using a wet cleaning process (See Application at page 4, lines 26-28 and Figure 2B at reference numeral 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate (See Application at page 5, lines 1-3 and Figure 2B at reference numerals 25, 11, 21 and 19), forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy (See Application at page 5, lines 7-8 and Figure 2B at reference numerals 27 and 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region (See Application at page 5, lines 20-24 and Figure 2C at reference numerals 11, 25 27, 29, 19 and 23), and cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose

a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 11, 25 27, 29, 19, 23 and 21), and whereby, the nickel silicide on the gate pattern is neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region, lumping of the nickel silicide is prevented, and a silicide residue is prevented from remaining on the spacers and the field region , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

Next, as set forth in claim 19, a method for fabricating a semiconductor device comprises forming a gate pattern and a source/drain region on a silicon substrate (See Application at page 4, lines 9-13, lines 20-21 and Figure 2A at reference numerals 19, 23 and 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed (See Application at page 5, lines 1-6 and Figure 2B at reference numerals 25, 11, 21, and 19), forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide (See Application at page 5, lines 7-8 and Figure 2B at reference numerals 27 and 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region (See Application at page 5, lines 20-24 and Figure 2C at reference numerals 25, 27, 29, 19 and 23), and selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 25, 27 and 29) and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-6 at reference numeral 25).

In addition, as set forth in claim 23, a method for fabricating a semiconductor device comprises forming a field region on a substrate to define an active region (See Application at page 4, lines 9-10 and Figure 2A at reference numerals 12 and 11), forming a gate pattern on the active region, wherein the gate pattern includes sidewalls (See Application at page 4, lines 11-14 and Figure 2A at reference numerals 19 and 13), forming spacers on the sidewalls of the gate pattern (See Application at page 4, lines 15-18 and Figure 2A at reference numerals 21 and 19), forming source/drain regions aligned with the spacers on both sides of the gate pattern (See Application at page 4, lines 20-21 and Figure 2A at reference numerals 21 and 19), cleaning the substrate using a wet cleaning process (See Application at page 4, lines 26-28 and Figure 2B at reference numeral 11), etching the silicon substrate using an RF sputter etching process to remove particles from the substrate (See Application on page 4, lines 29-30 and Figure 2B at reference numeral 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate (See Application at page 5, lines 1-3 and Figure 2B at reference numerals 25, 11, 21 and 19), forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy (See Application at page 5, lines 7-8 and Figure 2B at reference numerals 27 and 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region (See Application at page 5, lines 20-24 and Figure 2C at reference numerals 11, 25, 27, 29, 19 and 23), and cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region exposed (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 11, 25 27, 29, 19, 23 and 21), and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

Also, as set forth in claim 31, a method for fabricating a semiconductor device comprises forming a gate pattern and a source/drain region on a silicon substrate (See Application at page 4, lines 9-13, lines 20-21 and Figure 2A at reference numerals 19, 23 and 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed (See Application at page 5, lines 1-2, and Figures

2B at reference numerals 25, 11, 19 and 23), forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide (See Application at page 5, lines 7-8 and Figures 2B at reference numerals 27, 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region (See Application at page 5, lines 20-23 and Figure 2C at reference numerals 25, 27, 29, 19 and 23), and selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 25, 27, 29, and 23), and whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 5-6, 12, 16-17 and 27-31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,196,360 to Doan et al. ("the Doan patent") in view of U.S. Patent No. 5,766,997 to Takeuchi et al. ("the Takeeuchi patent") and U.S. patent Application Publication No. 2002/0151170A1 to Maex et al. ("the Maex publication").

B. Claims 2, 7-8, 13, 18-19, 22-23 and 26 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Doan with Takeuchi and Maex as applied to claims 1, 5-6, 12, 16-17 and 27-30 above, and further in view of U.S. Patent No. 6,503,840B2 to Catabay et al (hereinafter Catabay), U.S. Patent No. 6,664,166 B1 to Jaiswal et al (hereinafter Jaiswal) and U.S. Patent No. 6,775,046 B2 to Hill et al (hereinafter Hill).

7. ARGUMENTS

A. Claims 1, 5-6, 12, 16-17 and 27-31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,196,360 to Doan et al. ("the Doan patent") in view of U.S. Patent No. 5,766,997 to Takeuchi et al. ("the Takeeuchi patent") and U.S. patent Application Publication No. 2002/0151170A1 to Maex et al. ("the Maex publication").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference teaching. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Finally, the prior art reference must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the art and not based on applicant's disclosure. If an independent claim is non-obvious under section 103, then any claim depending therefrom is non-obvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The references of Doan, Takeuchi, Maex Catabay, Jaiswal and/or Hill cited by the Examiner, taken individually or in combination are legally insufficient for establishing a prima facie case of obviousness of the presently claimed invention as recited in claims 1, 2, 5-8, 12-13, 16-19, 22-23 and 26-31 under 35 U.S.C 103(a). Accordingly, it is respectfully requested that the Board reverse all rejections of claims 1, 2, 5-8, 12-13, 16-19, 22-23 and 26-31 under 35 U.S.C. 103(a).

(i) The teachings of the combination of Doan, Takeuchi and Maex at the very least fails to provide sufficient motivation to one skilled in the art to produce a method for fabricating a semiconductor device which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W,

Pt, Pd, V, Nb, or any combination thereof as essentially recited in claims 1, 12, 19, 23 and 31.

Claims 1, 12, 19, 23 and 31 recite, *inter alia*, a method for fabricating a semiconductor device which includes forming a Ni-based metal layer comprised of a nickel alloy for silicide and *wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.* (emphasis added).

As conceded by the Examiner in the Final Office Action, Doan fails to teach or suggest a method which includes forming a Ni-based metal layer comprised of a nickel alloy for silicide as recited in claims 1, 12, 19, 23 and 31. (See page 3 of the Final Office Action dated April 3, 2007). In addition, the Examiner also concedes that Doan and Takeuchi fail to teach or suggest a nickel alloy for silicide which includes any of the following materials Ta, Zr, Hf, Pt, Pd, V, Nb or any combination of these materials. (See page 5 of the Final Office Action dated April 3, 2007).

The Examiner attempts to cure the above-mentioned deficiencies of the Doan and Takeuchi by combining Doan, Takeuchi and Maex together in the manner set forth in the Final Office Action in an attempt to arrive at the methods recited in claims 1, 12, 19, 23 and 31. (See page 5 of the Final Office Action dated April 3, 2007). However, it is submitted that for at least the reasons set forth below, the Examiner has failed to meet his initial burden of establishing a prima facie showing of obviousness by failing to show that the above combination of cited reference provides sufficient motivation to one skilled in the art to provide a method for fabricating a semiconductor device which includes each and every element recited in claims 1, 12, 19, 23 and 31.

The Examiner appears to have interpreted the Takeuchi reference as teaching the formation of a nickel alloy for silicide. In particular, the Examiner appears to have interpreted the expression in Takeuchi of "...at least one kind of metal selected from a group tungsten (W), cobolt (Co), titanium (Ti) and nickel (Ni)" as sufficiently teaching the forming of a nickel alloy layer for silicide. (See page 3 of the Final Office Action dated April 3, 2007).

Applicants disagree with the Examiner's interpretation of the Takeuchi reference. Rather, the teachings of Takeuchi are insufficient for motivating one skilled in the art to form a nickel alloy for silicide as recited in claims 1, 12, 19, 23 and 31 because at the very least Takeuchi fails to specifically mention forming alloys anywhere in its disclosure. The fact that Takeuchi's mentions that a metal layer may formed using more than one type of metal in the same metal layer is still insufficient without more for teaching the use of alloys because as is well known in the art, metals may combined to form a metal layer without that metal layer necessarily being a metal alloy layer. (See Col. 7, lines 30-37 of Takeuchi). In other words, even when metals are mixed, alloys are not necessarily formed. Rather, additional steps are required for turning a mixture of metals into an alloy.

Takeuchi also fails to discuss any specific percentages or amounts for any of the metal consistuents in forming the first metal layer. As known in the art when forming an alloy, the specific percentages or amounts of the constituents of the alloy are typically stated. However, as discussed above, Takuchi is completely silent regarding any specific percentages or amounts for any of the metal consistuents in forming the metal layer and thus it is unclear from the teachings of Takeuchi whether an alloy is intended to be formed.

In sum, as can be gleaned from the above, Takeuchi teachings are insufficient for guiding or motivating one skilled in the art to form a nickel alloy for silicide as recited in claims 1, 12, 19, 23 and 31. Consequently, the Examiner's interpretation of Takeuchi is erroneous.

In addition, the Examiner's interpretation in the Final Office Action that the Maex reference cures the deficiency of the Doan and Takeuchi reference by teaching a nickel alloy for silicide which includes any of the following materials Ta, Zr, Hf, Pt, Pd, V, Nb or any combination of these materials is also erroneous for at least the reasons set forth below. Rather, the Maex reference does not cure the above noted deficiencies of the Doan and Takeuchi references because at the very least the teachings of the Maex reference fail to provide sufficient motivation to one skilled in the art for forming a Ni-based metal layer comprised of the nickel

alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in claims 1, 12, 19, 23 and 31.

Instead, contrary to the Examiner's position, Maex at best may provide motivation to form alloy layers which include nickel in amounts of less than 50%, more preferably less than 25%, more preferably less than 15%, even less than 10% and even as low as 1%. **(See paragraphs [0014], [0019] and [0082] of Maex).** Thus, based upon the above-mentioned teaching of Maex, one skilled in the art would likely not be motivated to form a nickel based alloy layer as required by claims 1, 12, 19, 23 and 31 but instead would likely only be motivated based upon the teachings of the Maex reference to form an alloy layer which was not nickel based and which included nickel in amounts of less than 50% down to about 1%.

Moreover, in addition to the reasons discussed above, there are other deficiencies with the Maex reference. Namely, substantially the entire disclosure of Maex is directed to cobalt compounds and cobalt alloys. Accordingly, one skilled in the art viewing the teaching of Maex would most likely be motivated form an alloy layer which included cobalt. Cobolt alloy layers are clearly different alloy layers than the specific nickel alloy layer recited in claims 1, 12, 19, 23 and 31 which do not include cobalt. Thus, the teachings of Maex even if combined with Doan and/or Takeuchi would still fail to motivate one skilled in the art to cure the above noted deficiencies of the Doan and Takeuchi references with regard to forming the specific nickel alloy layer recited in claims 1, 12, 19, 23 and 31.

Consequently, for at least the reasons set forth above, even if Doan and/or Takeuchi were modified based upon the teachings of Maex, this combination would not provide sufficient motivation to one skilled in the art to utilize a method of fabricating a semiconductor device which included forming a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in claims 1, 12, 19, 23 and 31. Thus, the combination of Doan and/or Takeuchi with Maex would still fail to teach or suggest all of the features recited in claims 1, 12, 19, 23 and 31.

Beeause the combination of Doan, Takeuchi and Maex fails to provide sufficient motivation to one skilled in the art to produce a method for fabricating a semiconductor device which includes each and every element recited in claims 1, 12, 19, 23 and 31, it is submitted that no *prima facie case* of obviousness has been established. Accordingly, the above rejections to claims 1, 12, 19, 23 and 31 and dependent claims 2, 5, 6, 16, 17 and 27-30 under 35 U.S.C. 103(a) should be reversed for at least the above reasons.

B. Claims 2, 7-8, 13, 18-19, 22-23 and 26 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Doan with Takeuchi and Maex as applied to claims 1, 5-6, 12, 16-17 and 27-30 above, and further in view of U.S. Patent No. 6,503,840B2 to Catabay et al (hereinafter Catabay), U.S. Patent No. 6,664,166 B1 to Jaiswal et al (hereinafter Jaiswal) and U.S. Patent No. 6,775,046 B2 to Hill et al (hereinafter Hill).

(i) The teachings of the combination of Doan, Takeuchi, and Maex with Catabay, Jaiswal and/or Hill fails to provide sufficient motivation to one skilled in the art to produce a method for fabricating a semiconductor device which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in claims 2, 7-8, 13, 18-19, 22-23 and 26.

As set forth above, the combination of Doan, Takeuchi and Maex fails to provide sufficient motivation to one skilled in the art to utilize a method of fabricating a semiconductor device which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in claims 2, 7-8, 13, 18-19, 22-23 and 26.

Furthermore, Catabay, Jaiswal and Hill references each fail to cure the above noted deficiencies of the Doan, Takeuchi and Maex references because at the very least Catabay, Jaiswal and Hill are each completely silent regarding a method of fabricating a semiconductor

device, which includes a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof , as essentially recited in claims 2, 7-8, 13, 18-19 and 26. Therefore, a combination of Doan Takeuchi and Maex with Catabay, Jaiswal and/or Hill fails to provide sufficient motivation to one skilled in the art to produce a method of fabricating a semiconductor device, which includes a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof , as essentially recited in claims 2, 7-8, 13, 18-19 and 26.

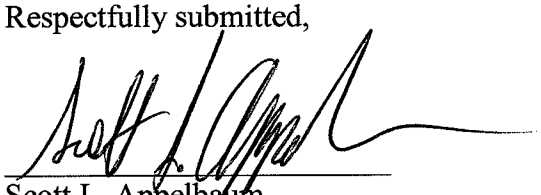
Because the combination of Doan, Takeuchi and Maex with Catabay, Jaiswal and/or Hill fails to provide sufficient motivation to one skilled in the art to produce a method for fabricating a semiconductor device which includes each and every element recited in claims 2, 7-8, 13, 18-19 and 26, it is submitted that no *prima facie case* of obviousness has been made. Accordingly, the above rejections to claims 2, 7-8, 13, 18-19 and 26,under 35 U.S.C. 103(a) should be reversed for at least the above reasons.

IV. CONCLUSION

The references of Doan, Takeuchi, Maex Catabay, Jaiswal and/or Hill cited by the Examiner, taken individually or in combination are legally insufficient for establishing a prima facie case of obviousness of the presently claimed invention as recited in claims 1, 2, 5-8, 12-13,

16-19, 22-23 and 26-31 under 35 U.S.C 103(a). Accordingly, it is respectfully requested that the Board reverse all rejections of claims 1, 2, 5-8, 12-13, 16-19, 22-23 and 26-31 under 35 U.S.C. 103(a).

Respectfully submitted,



Scott L. Appelbaum
Reg. No. 41,587
Attorney for Applicants

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797
Tel: (516) 692-8888
Fax: (516) 692-8889

CLAIMS APPENDIX

1. (previously presented) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region,

whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

2. (original) The method as claimed in claim 1, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

3. (canceled)

4. (canceled)

5. (original) The method as claimed in claim 1, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

6. (original) The method as claimed in claim 1, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

7. (original) The method as claimed in claim 1, further comprises etching the silicon substrate using an RF sputter stching process to remove particles from the substrate after forming the source/drain.

8. (original) The method as claimed in claim 7, wherein the RF sputter etching process comprises forming the Ni-based metal layer for silicide and the N-rich titanium nitride layer in-situ.

Claims 9-11 (Canceled)

12. (Previously presented) A method for fabricating a semiconductor device comprising:

forming a field region on a substrate to define an active region;

forming a gate pattern on the active region, wherein the gate pattern includes sidewalls;

forming spacers on the sidewalls of the gate pattern;

forming source/drain regions aligned with the spacers on both sides of the gate pattern;

cleaning the substrate using a wet cleaning process;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region,

whereby, the nickel silicide on the gate pattern is neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region,

lumping of the nickel silicide is prevented, and a silicide residue is prevented from remaining on the spacers and the field region , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

13. (original) The method as claimed in claim 12, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

14. (canceled)

15. (Canceled)

16. (original) The method as claimed in claim 12, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

17. (original) The method as claimed in claim 12, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

18. (original) The method as claimed in claim 12, further comprises etching the silicon substrate using an RF sputter etching process to remove particles from the substrate after forming the source/drain region.

19. (previously presented) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

20. (canceled)

21. (Canceled)

22. (Previously presented) The method as claimed in claim 19, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

23. (previously presented) A method for fabricating a semiconductor device comprising:

forming a field region on a substrate to define an active region;

forming a gate pattern on the active region, wherein the gate pattern includes sidewalls;

forming spacers on the sidewalls of the gate pattern;

forming source/drain regions aligned with the spacers on both sides of the gate pattern;

cleaning the substrate using a wet cleaning process;

etching the silicon substrate using an RF sputter etching process to remove particles from the substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region exposed , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

24. (canceled)

25. (canceled)

26. (previously presented) The method as claimed in claim 23, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

27. (previously presented) The method of claim 1, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

28. (previously presented) The method of claim 12, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

29. (previously presented) The method of claim 19, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

30. (previously presented) The method of claim 23, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

31. (previously presented) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region,

whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.